Amendments to the Claims

Claims 1-25 (Canceled).

26. (Previously Presented): Memory circuitry comprising:

a semiconductor substrate;

a plurality of word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer comprising at least a single well formed therein, the well comprising a base of said insulative layer received over the word lines, the insulative layer within which said well is formed peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within said single well over the word lines;

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array; and

the insulative layer has a substantially planar outermost surface, and the capacitors have inner capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

27. (Previously Presented): The memory circuitry of claim 26 wherein the insulative layer base of the well is substantially planar.

28. (Previously Presented): The memory circuitry of claim 26 wherein the word lines have insulative caps and the insulative layer base of the well has a lowest portion which is received at least 2000 Angstroms above the caps.

29. (Previously Presented): The memory circuitry of claim 26 comprising buried digit lines, the insulative layer base of the well having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

30. (Previously Presented): The memory circuitry of claim 26 comprising buried digit lines and wherein the insulative layer base of the well is substantially planar, and the insulative layer base of the well is received at least 1000 Angstroms above outermost tops of the digit lines.

Claim 31 (Canceled).

32. (Previously Presented): The memory circuitry of claim 26 wherein the inner capacitor storage node electrodes have topmost surfaces which are received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

Claims 33-53 (Canceled).

54. (Previously Presented): The memory circuitry of claim 26 wherein at least one of the inner storage node electrodes is spaced laterally inward of the outline peripherally defined by the well thereby forming a space between said one electrode and said outline.

Claims 55-57 (Canceled).

58. (Previously Presented): The memory circuitry of claim 26 wherein the memory cell storage capacitors respectively comprise an outer cell electrode having a topmost surface which is received elevationally outward of the insulative layer.

Claim 59 (Canceled).

60. (Previously Presented): The memory circuitry of claim 26 wherein the inner capacitor storage node electrodes respectively comprise a portion having a container shape.

61. (Previously Presented): The memory circuitry of claim 60 comprising openings formed in the insulative layer base of the well within which individual of the inner capacitor storage nodes are received, only part of the respective container-shaped portions being received within the respective openings.

62. (Previously Presented): The memory circuitry of claim 26 wherein the semiconductor substrate comprises bulk monocrystalline silicon.

63. (Previously Presented): The memory circuitry of claim 26 wherein the word lines comprise polysilicon.

64. (Previously Presented): The memory circuitry of claim 26 wherein the word lines comprise silicide.

65. (Previously Presented): The memory circuitry of claim 26 wherein the word lines comprise polysilicon and silicide.

66. (Previously Presented): The memory circuitry of claim 26 wherein the insulative layer comprises doped silicon dioxide.

67. (Previously Presented): The memory circuitry of claim 66 wherein the insulative layer comprises BPSG.

68. (Previously Presented): The memory circuitry of claim 66 wherein the insulative layer consists essentially of doped silicon dioxide.

69. (Previously Presented): The memory circuitry of claim 26 wherein the insulative layer has a thickness of from about 10,000 Angstroms to about 30,000 Angstroms.

70. (Previously Presented): The memory circuitry of claim 29 wherein the insulative layer base of the well has a lowest portion which is received less than 4000 Angstroms above outermost tops of the digit lines.

71. (Previously Presented): The memory circuitry of claim 26 comprising buried digit lines, the insulative layer base of the well having a lowest portion which is received from about 2500 Angstroms to about 3000 Angstroms above outermost tops of the digit lines.